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EXAMINER	
TORRES, JOSEPH D	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/848,218	Applicant(s) MAEDA ET AL.	
	Examiner Joseph D. Torres	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 January 1950*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) *See Continuation Sheet* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,12,16,20,24,31,35,39,43 and 47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20041208*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims withdrawn from consideration are 3-11,13-15,17-19,21-23,25-30,32-34,36-38,40-42,44-46 and 48-50.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1, 2, 12, 16, 20, 24, 31, 35, 39, 43 and 47, drawn to An error correction device comprising: **a buffer memory for storing at least one sector of data having a structure where each of N words of error correcting code comprises a data unit, an inner code parity unit, and one error detecting code**; a syndrome calculating means for generating syndrome for data read from said buffer memory; an error correcting means for correcting error-containing data in said buffer memory by detecting an error position from the syndrome generated by said syndrome calculating means and by calculating an error value; an error detecting means for detecting an error, one sector at a time, in error-corrected data generated by said error correcting means; **a storing means for storing mid-term results, in code word units, of an error detecting process in said error detecting means**; a bus control means for controlling data transfer between said buffer memory, said syndrome calculating means, said error correcting means, and said error detecting means; and a system control means for performing various processes for error correction in predetermined procedures a necessary number of times, wherein said bus control means comprises: a before-syndrome

data transfer sub means for transferring data to be corrected from said buffer memory to said syndrome calculating means and to said error detecting means concurrently in code word units until said syndrome calculating means detects an error-containing code; **an after-syndrome data transfer sub means for, when said syndrome calculating means detects an error-containing code, transferring subsequent data in said buffer memory only to said syndrome calculating means in code word units**; and an error-detecting data transfer sub means for, after said error correcting means corrects an error contained in data in said buffer memory based on the syndrome transmitted by said syndrome calculating means, **transferring error-corrected data which include the code word from which the error-containing code has been detected up to and including a final code word from said buffer memory to said error detecting means in code word units for error detection; said error detecting means comprises**: a parallel process sub means for, until said syndrome calculating means detects an error-containing code, storing the mid-term results of the error detecting process to said storing means in code word units, and executing error detection of a code word transmitted from said buffer memory in parallel with syndrome calculation done by said syndrome calculating means; and **an after-correction error detecting sub means for, after said syndrome calculating means detects an error-containing code, executing error detection for data**

transferred from said buffer memory after the error correction done by said error correcting means, following a code word which has previous contents before the occurrence of an error and which is already stored in said storing means, classified in class 714, subclass 769.

II. Claims 3 and 4, drawn to An error correction device comprising: a buffer memory for storing at least one sector of data having a structure where each of N words of error correcting code comprises a data unit, an inner code parity unit, and one error detecting code; a syndrome calculating means for generating syndrome for data read from said buffer memory; an error correcting means for correcting error-containing data in said buffer memory by detecting an error position from the syndrome generated by said syndrome calculating means and by calculating an error value; an error detecting means for detecting an error, one sector at a time, in error-corrected data generated by said error correcting means; a bus control means for controlling data transfer between said buffer memory, said syndrome calculating means, said error correcting means, and said error detecting means; and a system control means for performing various processes for error correction in predetermined procedures a necessary number of times; wherein said bus control means comprises: a concurrent data transfer sub means for transferring data to be corrected from said buffer memory to said syndrome calculating means and to said error

detecting means concurrently in code word units until said syndrome calculating means detects an error-containing code; and an error-detecting data transfer sub means for, only when said syndrome calculating means has detected an error-containing code, after the error correction done by said error correcting means, **transferring data in a sector containing error-corrected data in and after the code word from which the error-containing code has been detected**, from said buffer memory to said error detecting means for error detection, said error detecting means comprises: a parallel error detecting sub means for executing error detection for a code word transmitted from said buffer memory, in parallel with the syndrome calculation done by said syndrome calculating means; and **an error re-detecting sub means for, only when said syndrome calculating means has detected an error-correcting code, executing error detection one more time for the error-corrected data**, classified in class 714, subclass 755.

III. Claims 5 and 6, drawn to An error correction device comprising: a buffer memory for storing at least one sector of data having a structure where each of N words of error correcting code comprises a data unit, an inner code parity unit, and one error detecting code; a syndrome calculating means for generating syndrome for data read from said buffer memory; an error correcting means for correcting error-containing data in said buffer memory by detecting an error position from the syndrome generated by

said syndrome calculating means and by calculating an error value; an error detecting means for detecting an error, one sector at a time, in error-corrected data generated by said error correcting means; a storing means for storing mid-term results, in code word units, of an error detecting process in said error detecting means; a bus control means for controlling data transfer between said buffer memory, said syndrome calculating means, said error correcting means, and said error detecting means; and a system control means for performing various processes for error correction in predetermined procedures a necessary number of times, wherein said bus control means comprises: a first transfer sub means for executing a first transfer where data to be corrected are transferred in code word units from said buffer memory concurrently to said syndrome calculating means and to said error detecting means until said syndrome calculating means detects an error-containing code, and **for suspending the first transfer when said syndrome calculating means has detected an error-containing code**; and **a second transfer sub means for executing a second transfer where a code word from which an error has been detected and corrected is transferred from said buffer memory to said error detecting means after the error correction done by said error correcting means, based on the syndrome transmitted from said syndrome calculating means; and a first transfer resuming sub means for, after the completion of the second transfer, making**

the first transfer sub means resume the first transfer for subsequent code words including the code word which has been subjected to the second transfer, and said error detecting means comprises: a first error detecting sub means for, until said syndrome calculating means detects an error-containing code, executing a first error detection where error detection is performed for a code word transmitted from said buffer memory in parallel with the syndrome calculation done by said syndrome calculating means, while storing mid-term results of the error detection in code word units to said storing means; **a second error detecting sub means for, after said syndrome calculating means detects an error-containing code, executing a second error detection where error detection is resumed for code words whose errors have been detected and corrected by said error correcting means, starting at a code word which has previous contents before the occurrence of an error and which is already stored in said storing means**; and a first error detection resuming sub means for, after the completion of the second error detection for the error-corrected code word, making the first error detecting sub means resume the first error detection for subsequent code words, classified in class 714, subclass 708.

IV. Claims 7-11, 13-15, 17-19, 21-23, 25-27, 32-34, 36-38, 40-42, 44-46, and 48-50, drawn to An error correction device comprising; a buffer memory for storing at least one ECC block of data having a structure where a

plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to error correction; a syndrome calculating means for generating syndrome for data read from said buffer memory; an error correcting means for correcting error-containing data in said buffer memory by detecting an error position from the syndrome generated by said syndrome calculating means and by calculating an error value; an error detecting means for detecting an error in error-corrected data generated by said error correcting means; a bus control means for controlling data transfer between said buffer memory, said syndrome calculating means, said error correcting means, and said error detecting means; and a system control means for performing various processes for error correction in predetermined procedures a necessary number of times, wherein said system control means comprises: a first-time error correction sub means for reading data from said buffer memory in a same direction as calculation for an error detecting code as a first-time error correction; for transferring the read data to said syndrome calculating means and to said error detecting means concurrently until said syndrome calculating means

detects an error-containing code; **for making said syndrome calculating means execute syndrome calculation and said error detecting means execute error detection in parallel; for making said error correcting means execute error correction when said syndrome calculating means has detected an error-containing code; and for making one of said syndrome calculating means and said error correcting means provide the system control means with information which designates a code word containing the error-containing code; an even-numbered error correction sub means for reading a code word in a different direction from a preceding odd-numbered error correction; for transferring the code word to said syndrome calculating means and to said error detecting means concurrently until said syndrome calculating means detects an error-containing code; for making said syndrome calculating means execute syndrome calculation and said error detecting means execute error detection in parallel; for making said error correcting means execute error correction when said syndrome calculating means detects an error-containing code; and for making said error correcting means provide said system control means with information which designates the position of the error-containing code in an error correcting code word obtained in the error correction; a non-error range designating sub means for designating, one sector at a time, a range from which an error-**

containing code has not been detected at the odd-numbered error correction or the subsequent even-numbered error correction, based on said information that designates the code word including the error-containing code and said information that designates the position of the error-containing code in the error correcting code word; an odd-numbered error correction sub means for, as an odd-numbered error correction as a third-time or later error correction, providing concurrently said syndrome calculating means and said error detecting means with a code in the same direction as in the previous odd-numbered error correction except for a sector in one ECC block which has been designated by said non-error range designating sub means as the range from which an error-containing code has not been detected in and before the preceding even-numbered error correction until said syndrome calculating means detects an error-containing code; for making said syndrome calculating means execute syndrome calculation and said error detecting means execute error detection in parallel; for making said error correcting means execute error correction when said syndrome calculating means detects an error-containing code; and for making one of said syndrome calculating means and said error correcting means provide said system control means with information which designates the code word including the error-containing code; and a

number-of-times control sub means for repeating the odd-numbered error correction and the even-numbered error correction a predetermined number of times, classified in class 714, subclass 785.

V. Claims 28 and 29, drawn to An error correction device which performs error correction for data in ECC blocks each having a structure where error correcting code words each comprising a data unit and a parity unit are arranged in vertical and horizontal directions so as to realize repeated error correction, and predetermined data composed of a predetermined number of code words in the vertical or horizontal direction (data in the horizontal direction are referred to as sector) are as one unit subjected to error correction, and which also perform syndrome calculation and error detection in parallel with a storage of demodulated codes in a buffer memory, said error correction device comprising: a first syndrome calculating means for performing syndrome calculation with said buffer memory a first error detecting means which pairs up with the first syndrome calculating means; a second syndrome calculating means for performing syndrome calculation of demodulated codes without said buffer memory; a second error detecting means which pairs up with the second syndrome calculating means a storing means for storing mid-term results of calculations of the first error detecting means and the second error detecting means; a buffer memory parallel transfer means for transferring data transmitted from upstream to the second syndrome calculating

means and to the second error detecting means in parallel with storage of the data in said buffer memory until the second syndrome calculating means detects an error-containing code; **an error-detecting means switch means for switching between the first error detection means and the second error detection means in a manner that after the second syndrome calculating means detects an error-containing code, said storing means is provided with the mid-term results of the calculation by the second error detecting means of code words until said error- containing code is detected, and on and after the second-time error correction in a same direction, after the second syndrome calculating means detects an error- containing code, said storing means is provided with the mid-term results of the calculation by the second error detecting means of code words until said error- containing code is detected an error correcting means for performing error correction after one of the first error detecting means and the second error detecting means detects an error-containing code word a parallel transfer means for, on and after the second-time error correction in the same direction, before the first syndrome calculating means detects an error-containing code, transferring data stored in said buffer memory, starting at a code word which is not stored in said storing means to the first syndrome calculating means and to the first error detecting means and a**

second-time onward detecting-processed data use means for, on and after the second-time error detection in the same direction done by the second error detecting means, performing error detection of the subsequent code words by using the mid-term results stored in said storing means, classified in class 714, subclass 774.

VI. Claim 30, drawn to An error correction device which performs error correction for data in a plurality of ECC blocks each having a structure where error correcting code words each comprising a data unit and a parity unit are arranged in vertical and horizontal directions so as to realize repeated error correction, and predetermined data composed of a predetermined number of code words in the vertical or horizontal direction (data in the horizontal direction are referred to as sector) are as one unit subjected to concurrent or parallel error correction by pipeline processing, and which also perform syndrome calculation and error detection in parallel with a storage of demodulated codes in a buffer memory, said error correction device comprising: a buffer memory for storing ECC blocks to be processed in pipeline, on a block-by-block basis; a first syndrome calculating means for performing syndrome calculation a first error detecting means which pairs up with the first syndrome calculating means a second syndrome calculating means for performing syndrome calculation; a storing means for storing the mid-term results of the calculation done by the first error detecting means and the second error

detecting means in predetermined data units of the ECC blocks in process such as ECC block units, sector units, or sector group units; **a demodulated-code calculation selecting means for making one of the first syndrome calculating means and the second syndrome calculating means execute syndrome calculation for demodulated data transmitted from upstream, and making the other syndrome calculating means execute syndrome calculation when there are data stored in said buffer memory a buffer memory parallel transfer means for, before the syndrome calculating means selected by said demodulated-code calculation selecting means detects an error containing code, sequentially transferring data from upstream to the syndrome calculating means and the error detecting means which pairs up therewith, and at the same time storing the data in said buffer memory> an error-detecting-means switch means for switching between the first error detection means and the second error detection means in a manner that after the syndrome calculating means selected by said demodulated -code calculation selecting means detects an error-containing code in data transmitted from upstream in said data units, said storing means is provided with the mid-term results of the calculation by the corresponding error detecting means of code words until said error-containing code is detected, and on and after the second-time error correction in a**

same direction, after the corresponding second syndrome calculating means detects an error -containing code, said storing means is provided with the mid-term results of the calculation by the corresponding error detecting means of code words until said error-containing code is detected an error correcting means for performing error correction after the first error detecting means or the second error detecting means detects an error -containing code word a stored code calculation selecting means for selecting between the first syndrome calculating means and the second syndrome calculating means in ECC block units or in said data units so as to perform syndrome calculation for the data stored in said buffer memory a parallel transfer means for, on and after the second-time error correction in a same direction, before the first syndrome calculating means detects an error -containing code in said data units, transferring code words not stored in said storing means out of data stored in said buffer memory to the corresponding one of the first syndrome calculating means and the first error detecting means; a second-time onward detecting-processed data use means for, on and after the second-time error detection in the same direction done by the corresponding error detecting means, performing error detection of the subsequent code words in said data units by using the mid-term results stored in said storing means

a means-basis pipeline processing notification means for transmitting ECC blocks which have been subjected to error correction downstream for storing ECC blocks to be processed next to said buffer memory and for making the storage known to said stored code calculation selecting means, said buffer- memory parallel transfer means, said error-detecting-means switch means, the first syndrome calculating means, the second syndrome calculating means, said error detecting means; said error correcting means, said parallel transfer means, and said second-time onward detecting-processed data use means and a system control means for controlling a data transfer and data rewriting of ECC blocks in process in ECC block units or said data units at each means and for coordinating with other means the transfer of error-corrected ECC blocks downstream and the storage of new ECC blocks to be processed in said buffer memory, classified in class 714, subclass 776.

The inventions are distinct, each from the other because of the following reasons: Inventions Group I and Groups II-VI are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together and they have different modes of operation, different functions, or different effects (MPEP § 806.04, MPEP § 808.01). In the instant case the different inventions the applicant does not disclose that the different aspects exemplified by the claims can be used together and each of

Groups II-VI have different functions (highlighted in the previous paragraphs) from Group I (also, highlighted in the previous paragraphs).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Groups II-VI, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Groups II-VI is not required for Group I, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation with Robert N. Wieland on 12/7/2004 a provisional election was made with traverse to prosecute the invention of Group I, claims 1, 2, 12, 16, 20, 24, 31, 35, 39, 43 and 47. Affirmation of this election must be made by applicant in replying to this Office action. Claims 3-11, 13-15, 17-19, 21-23, 25-30, 32-34, 36-38,

40-42, 44-46, and 48-50 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 'a1' to 'a12' in Figure 4; 'b1' to 'b12' in Figure 6; 'c1' to 'c12' in Figure 10; '812' in Figure 12; and 'e1' to 'e11' in Figure 4. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the

examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "5" and "7" have both been used to designate the same block in Figure 11. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "9" has been used to designate both an Downstream Process Unit and a Transfer Control Unit. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the

page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "10" has been used to designate both an Upstream Process Unit and a Demodulator. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The Examiner asserts that the drawings are replete with errors some of which the Examiner has pointed out, above. The Applicant should review the drawings and the specification to make corrections to ensure all the reference numerals in the drawings are in the specification and all the reference numerals in the specification are in the drawings. In addition, the Applicant should review the drawings to make sure that

different reference numerals are not used to designate the same object and to make sure that the same reference numeral is not used to designate distinct objects.

Specification

3. The abstract of the disclosure is objected to because the definite article "the" where no antecedent basis is provided rendering the abstract confusing (Note: using the definite article "the" where no antecedent basis, implies that the reader must look outside of the abstract for antecedent basis). Correction is required. See MPEP § 608.01(b).

Claim Objections

4. Claim 1 is objected to because of the following informalities: claim 1 is not properly indented, that is, "a buffer memory ..." in line 1 should start a new line and be properly indented (Note: "an error correcting..." in line 5, "an error deetecing..." in line 8, etc. should also start a new line and be properly indented). In addition, "a before-syndrome..." in line 18, "an after-syndrome..." in line 18, etc. should be twice indented.
Claim 1 recites "a syndrome calculating means for generating syndrome for data read from said buffer memory". The term "generating syndrome" should be revised, i.e., --generating **a** syndrome--.
Claim 1 recites, "transferring error-corrected data which include the code word from which the error-containing code has been detected up to and including a final code

word", which needs to be rewritten in grammatically correct English ensuring that verbs are properly conjugated and removing any ambiguity in the phrase.

Appropriate correction is required.

Claim 1 recites, "an after-correction error detecting sub means for, after said syndrome calculating means detects an error-containing code, executing error detection for data transferred from said buffer memory after the error correction done by said error correcting means, following a code word which has previous contents before the occurrence of an error and which is already stored in said storing means", which needs to be rewritten in grammatically correct English removing any ambiguity in the phrase.

Claim Rejections - 35 USC § 112

5. Claims 1, 2, 12, 16, 20, 24, 31, 35, 39, 43 and 47 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites, "one sector of data having a structure where each of N words of error correcting code comprises a data unit". N is undefined in the claim. The term "having a structure" is indefinite.

Claim 1 recites, "an error detecting means for detecting an error, one sector **at a time**" [Emphasis added]. The term "at a time" is indefinite since it is not related to the timing structure of error correction device.

Claim 1 recites, "a storing means for storing mid-term results, in code word units, of an error detecting process in said error detecting means", which is open to may

interpretations, hence indefinite. The following is a short list to some of the interpretations for the sentence: 1. --a storing means of an error detecting process in said error detecting means for storing mid-term results, in code word units--, 2. --a storing means for storing mid-term results of an error detecting process in said error detecting means, in code word units--, 3. --a storing means for storing mid-term results of an error detecting process, in code word units, in said error detecting means--, 4. --a storing means in said error detecting means for storing mid-term results of an error detecting process, in code word units--, etc.

Claim 1 recites, "performing various processes for error correction in predetermined procedures a necessary number of times". The term "various processes" is indefinite since various is indefinite since various processes are a process and there is nothing definite about the various processes to distinguish them from each other. The term "a necessary number of times" is indefinite since it would be impossible for one of ordinary skill in the art at the time the invention was made to determine the necessary number of times since "necessary" is not linked to any definite attribute of an error correction device.

Claim 1 recites the limitation "the code word" in line 29. There is insufficient antecedent basis for this limitation in the claim.

Claim 1 recites, "transferring error-corrected data which include the code word from which the error-containing code has been detected up to and including a final code word", which is indefinite since it has various interpretations as listed: 1. --transferring error-corrected data up to and including a final code word, the error-corrected data

including the code word from which the error-containing code has been detected--, 2. --transferring error-corrected data which includes the code word from which the error-containing code has been detected up, whereby the error-containing code has been detected up to and including a final code word-- and 3. --transferring error-corrected data the error-corrected data which includes the code word up to and including a final code word from which the error-containing code has been detected--

Claim 1 recites the limitation "the error correction" in lines 42-43. There is insufficient antecedent basis for this limitation in the claim.

Claim 1 recites the limitation "the occurrence of an error" in line 44. There is insufficient antecedent basis for this limitation in the claim.

Claim 1 recites, "an after-correction error detecting sub means for, after said syndrome calculating means detects an error-containing code, executing error detection for data transferred from said buffer memory after the error correction done by said error correcting means, following a code word which has previous contents before the occurrence of an error and which is already stored in said storing means", which is incomprehensible and has to be rewritten in grammatically correct English. In particular, little sense can be made out of the phrase, "following a code word which has previous contents before the occurrence of an error and which is already stored in said storing mean". Note: errors occur during transmission not during decoding; decoding only detects the errors that occurred during transmission.

Claims 1, 2, 12, 16, 20, 24, 31, 35, 39, 43 and 47 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. Claim 1 recites, "one sector of data having a structure where each of N words of error correcting code comprises a data unit". The relationship between a sector and N words of error correcting code is missing. In particular, the term "having a structure" is indefinite.

Claim 1 recites, "an error detecting means for detecting an error, one sector **at a time**" [Emphasis added]. The relationship between the timing structure of the error correction device is missing, hence it is unclear what is meant by "one sector at a time".

Claim 1 recites, "a storing means for storing mid-term results, in code word units, of an error detecting process in said error detecting means". The relationship between "code word units" and the sector, the data unit, the inner code parity unit and the one error detecting code is missing.

Claim 1 recites, "performing various processes for error correction in predetermined procedures a necessary number of times". The relationship between processes and procedures is missing, i.e., is each process a procedure, is there more than one process for each procedure or are all of the processes loosely associated with all of the procedures?

Line 21 of claim 1 recites, "error containing code" whereas line 6 of claim 1 recites "error containing data". The relationship "error-containing data" and "error containing code" is

missing. The relationship between "error containing code" and the sector, the data unit, the inner code parity unit and the one error detecting code is missing.

Claim 1 recites, "following a code word which has previous contents before the occurrence of an error and which is already stored in said storing means". It is unclear what a "previous contents" has to do with "the occurrence of an error" or any of the other data structures recited in claim 1.

The Examiner would like to point out that claim 1, 2, 12, 16, 20, 24, 31, 35, 39, 43 and 47 are replete with 112 issues and need to be rewritten in grammatically correct English. Claims 2, 12, 16, 20, 24, 31, 35, 39, 43 and 47 have similar 112 problems as in claim 1. The Examiner suggests that the Applicant make use of a competent translator in rewriting the claims since the claims appear to be directly translated from a foreign language. The Applicant with the use of a competent translator should also review claims 2, 12, 16, 20, 24, 31, 35, 39, 43 and 47 for errors and revise all of the claims using the previous paragraphs as guidelines for rewriting the claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1, 2, 12, 16, 20, 24, 31, 35, 39, 43 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zook; Christopher P. (US 5592498 A, hereafter referred to as Zook '498) in view of Zook; Christopher P. (US 5991911 A, hereafter referred to as Zook '911).

35 U.S.C. 103(a) rejection of claims 1, 2, 12, 16, 20, 24, 31, 35, 39, 43 and 47.

Zook '498 teaches an error correction device comprising: a buffer memory for storing at least one sector of data having a structure where each of N words of error correcting code comprises a data unit, a code parity unit, and one error detecting code (Buffer 15 in Figure 1 of Zook '498 is a buffer memory for storing at least one sector of data having a structure where each of N words of error correcting code comprises a data unit, a code parity unit, and one error detecting code); a syndrome calculating means for generating syndrome for data read from said buffer memory (Generator 20 in Figure 1 of Zook '498 is a syndrome calculating means for generating syndrome for data read from said buffer memory); an error correcting means for correcting error-containing data in said buffer memory by detecting an error position from the syndrome generated by

said syndrome calculating means and by calculating an error value (Corrector 60 in Figure 1 of Zook '498 is an error correcting means for correcting error-containing data in said buffer memory by detecting an error position from the syndrome generated by said syndrome calculating means and by calculating an error value); an error detecting means for detecting an error, one sector at a time, in error-corrected data generated by said error correcting means; a storing means for storing mid-term results, in code word units, of an error detecting process in said error detecting means (EDC/CRC Checker 70 in Figure 1 of Zook '498 is an error detecting means for detecting an error, one sector at a time, in error-corrected data generated by said error correcting means; a storing means for storing mid-term results, in code word units, of an error detecting process in said error detecting means); a bus control means for controlling data transfer between said buffer memory, said syndrome calculating means, said error correcting means, and said error detecting means (Controller 10 in Figure 1 of Zook '498 is a bus control means for controlling data transfer between said buffer memory, said syndrome calculating means, said error correcting means, and said error detecting means); and a system control means for performing various processes for error correction in predetermined procedures a necessary number of times, wherein said bus control means comprises: a before-syndrome data transfer sub means for transferring data to be corrected from said buffer memory to said syndrome calculating means and to said error detecting means concurrently in code word units until said syndrome calculating means detects an error-containing code; an after-syndrome data transfer sub means for, when said syndrome calculating means detects an error-containing code,

transferring subsequent data in said buffer memory only to said syndrome calculating means in code word units; and an error-detecting data transfer sub means for, after said error correcting means corrects an error contained in data in said buffer memory based on the syndrome transmitted by said syndrome calculating means, transferring error-corrected data which include the code word from which the error-containing code has been detected up to and including a final code word from said buffer memory to said error detecting means in code word units for error detection; said error detecting means comprises: a parallel process sub means for, until said syndrome calculating means detects an error-containing code, storing the mid-term results of the error detecting process to said storing means in code word units, and executing error detection of a code word transmitted from said buffer memory in parallel with syndrome calculation done by said syndrome calculating means; and an after-correction error detecting sub means for, after said syndrome calculating means detects an error-containing code, executing error detection for data transferred from said buffer memory after the error correction done by said error correcting means, following a code word which has previous contents before the occurrence of an error and which is already stored in said storing means (Controller 10 in Figure 1 of Zook '498 is a system control means **capable of** performing various processes for error correction in predetermined procedures a necessary number of times, wherein said bus control means comprises: a before-syndrome data transfer sub means **capable of** transferring data to be corrected from said buffer memory to said syndrome calculating means and to said error detecting means concurrently in code word units until said syndrome calculating means detects

an error-containing code; an after-syndrome data transfer sub means **capable of**, when said syndrome calculating means detects an error-containing code, transferring subsequent data in said buffer memory only to said syndrome calculating means in code word units; and an error-detecting data transfer sub means **capable of**, after said error correcting means corrects an error contained in data in said buffer memory based on the syndrome transmitted by said syndrome calculating means, transferring error-corrected data which include the code word from which the error-containing code has been detected up to and including a final code word from said buffer memory to said error detecting means in code word units for error detection; said error detecting means comprises: a parallel process sub means **capable of**, until said syndrome calculating means detects an error-containing code, storing the mid-term results of the error detecting process to said storing means in code word units, and executing error detection of a code word transmitted from said buffer memory in parallel with syndrome calculation done by said syndrome calculating means; and an after-correction error detecting sub means **capable of**, after said syndrome calculating means detects an error-containing code, executing error detection data transferred from said buffer memory after the error correction done by said error correcting means, following a code word which has previous contents before the occurrence of an error and which is already stored in said storing means, see, e.g., In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997) and In re Swinehart, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971)).

However Zook '498 does not explicitly teach the specific use of an inner code parity unit.

Zook '911, in an analogous art, teaches a product code which is comprised of inner and outer parity.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Zook '498 with the teachings of Zook '911 by including use of an inner code parity unit. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of an inner code parity unit would have provided the opportunity to increase error tolerance (col. 3, lines 26-28, Zook '911).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Primary Examiner
Art Unit 2133